CLAIMS

[Claim 1] A semiconductor storage device comprising:

a. a memory cell array including a plurality of word lines;

b. a refresh element configured to generate a request for refresh and sequentially generating refresh addresses;

c. an address selector adapted to select an access address in response to a request for access, said address selector selecting a refresh address from a plurality of generated refresh addresses in response to the request for refresh;

d. a word line selector adapted to select a word line from the plurality of word lines in response to the address selected by said address selector; and

e. a selection disable element for stopping the address selection performed by said address selector while the access or the refresh is being performed in said memory cell array.

[Claim 2] The semiconductor storage device according to Claim 1, wherein said memory cell array is divided into a plurality of blocks, the semiconductor storage device further comprising a block selection element configured to select a block from said plurality of blocks in response to the address selected by said address selector, said selection disable element stopping said address selector from performing address selection while the access or the refresh is being performed on the block selected by said block selection element.

[Claim 3] The semiconductor storage device according to Claim 2, wherein said word line selector sequentially selects all the word lines one after another with respect to each of said blocks in response to the refresh address selected by said address selector.

[Claim 4] The semiconductor storage device according to Claim 3, wherein said selection disable element further comprises:

a busy signal generation circuit configured to assert a busy signal in response to the request for the access or the refesh, and disabling the busy signal after the access or the refresh on the block selected by said block selection element is completed, and said address selector includes:

an input device adapted to input the access address in response to the request for the access and input the refresh address in response to the request for the refresh; and

a latch element for capturing the input address after the busy signal is disabled.

[Claim 5] The semiconductor storage device according to Claim 4, wherein said busy signal generation circuit includes:

a busy signal line provided in common through said plurality of blocks;

a charge device for charging said busy signal line in response to the request for the refresh;

a discharge device provided in correspondence with each of said plurality of blocks, said discharge device discharging said busy signal line after the access or the refresh on the corresponding block is completed.

[Claim 6] A refresh method for a semiconductor storage device having a memory cell array including a plurality of word lines, said method comprising the steps of:

making a request for refresh and sequentially generating refresh addresses;

selecting an access address in response to a request for access, and selecting a refresh address from the refresh addresses in response to the request for refresh;

selecting a word line from the word lines in response to the selected address; and

stopping the selection from the access addresses and the refresh addresses after the access or the refresh is being performed in the memory cell array.

[Claim 7] The refresh method for a semiconductor storage device according to Claim 6, wherein the memory cell array is divided into a plurality of blocks, said refresh method further comprising a step of selecting a block from the blocks in response to the selected address, said stopping step including stopping the selection from the access addresses and the refresh addresses after the access or the refresh on the selected block is being performed.

[Claim 8] The refresh method for a semiconductor storage device according to Claim 7, wherein said selecting step includes selecting all the word lines one after another with respect to each of the blocks in response to the refresh address.

[Claim 9] The refresh method for a semiconductor storage device according to Claim 8, wherein said stopping step includes:

a busy signal generation step of asserting a busy signal in response to the request for the access or the refresh, and disabling the busy signal after the access or the refresh on the selected block is completed, and said selecting step includes the steps of:

inputting the access address in response to the request for the access;

inputting the refresh address in response to the request for the refresh; and

capturing and latching the input address after the busy signal is disabled.

[Claim 10] The refresh method for a semiconductor storage device according to Claim 9, wherein the semiconductor storage device further has a busy signal line provided in common through the plurality of blocks, said busy signal generation step includes:

charging the busy signal line in response to the request for the access or the refresh;

discharging the busy signal line after the access or the refresh on the corresponding block is completed.